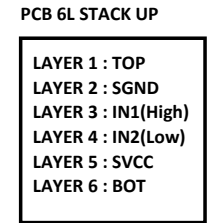


Volks DIS/UMA (14"/15.6") Ultra/Slim Intel Chief River Platform Block Diagram



BQ24738
System Charge Power (+BATCHG)

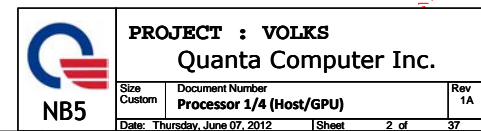
Richtek RT8223P
System Power (+3VPCU/+5VPCU/
+3VS5/+5VS5)

**NCP6132/NCP5911/RT8240P/
TP551462RGER**
Processor Power (+VCC_CORE/
+1.5_VTT/+VCCSA)

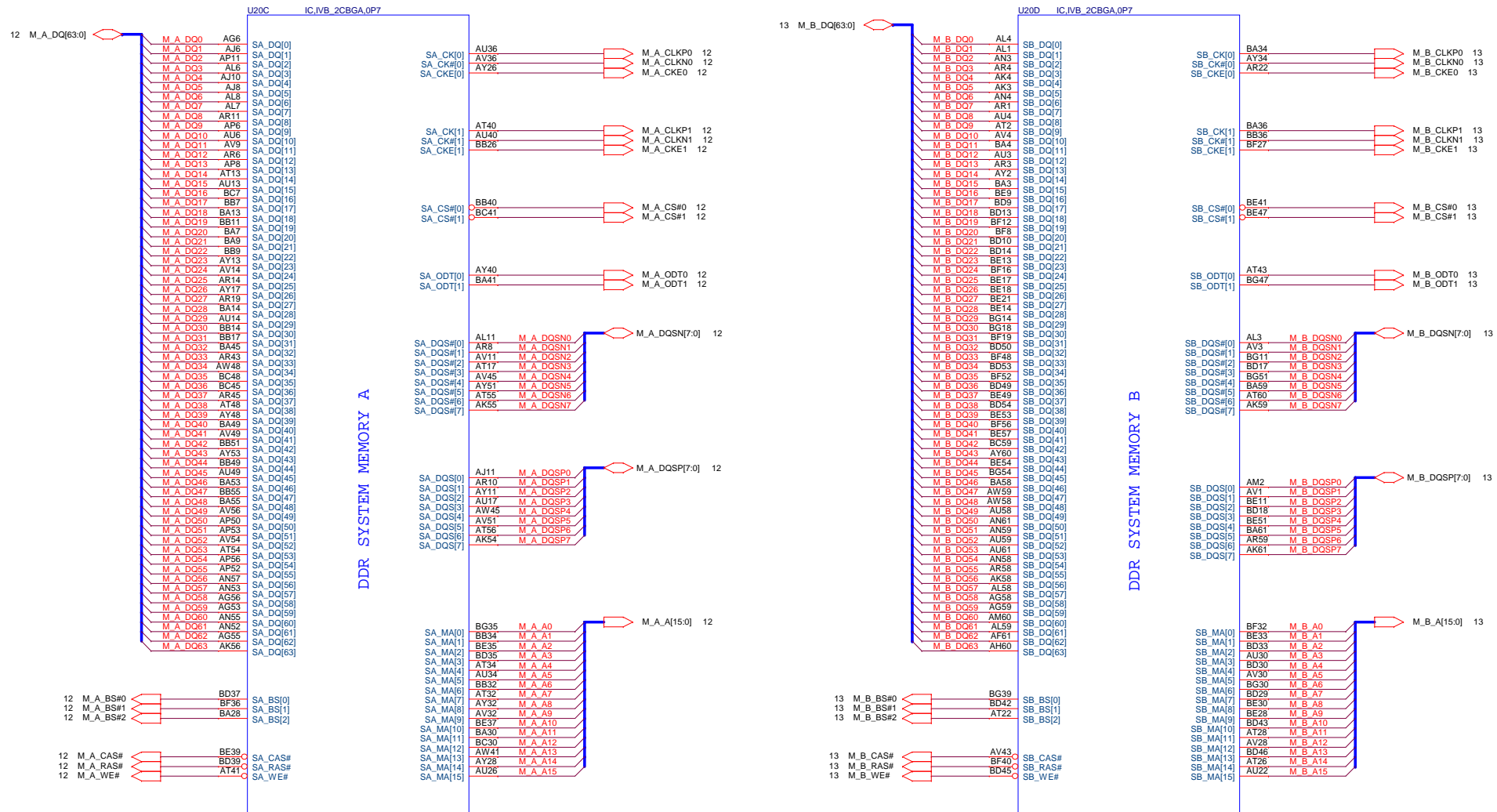
SLG55448V
System Discharge Power
(+1.5V/+3V/+5V)

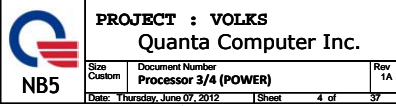
Richtek RT8207
System Memory Power (+1.5VSUS/
+0.75V_DDR_VTT)

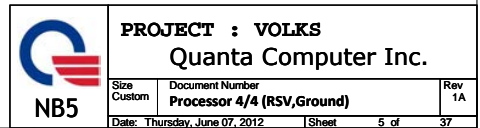
NCP3218G
GPU core power(+VGACORE)

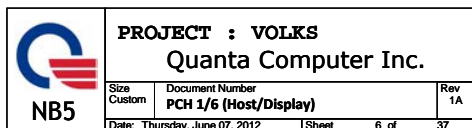


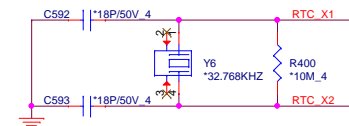
Ivy Bridge Processor (DDR3)



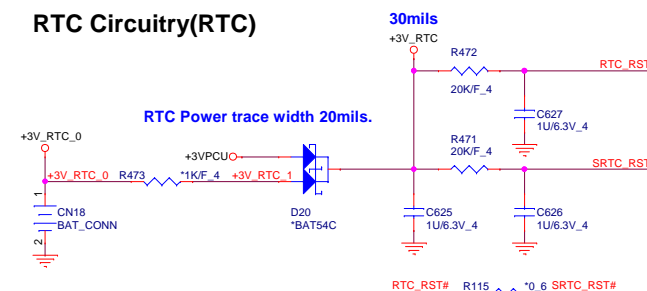




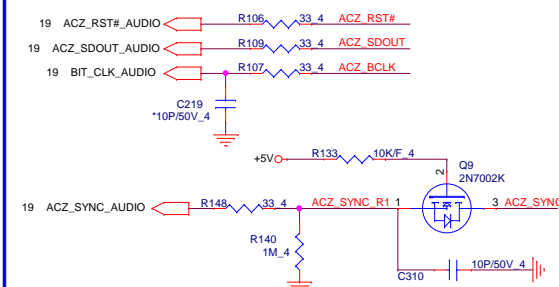




no stuff If use green Clock

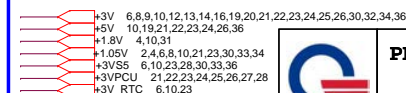
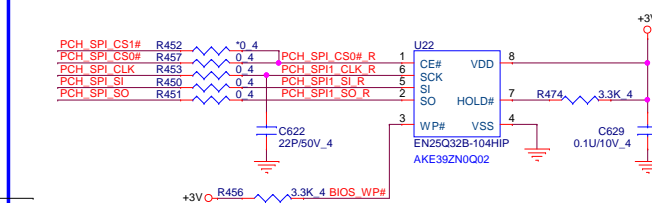



HDA Bus(CLG)



☐ PCH SPI ROM(CLG)

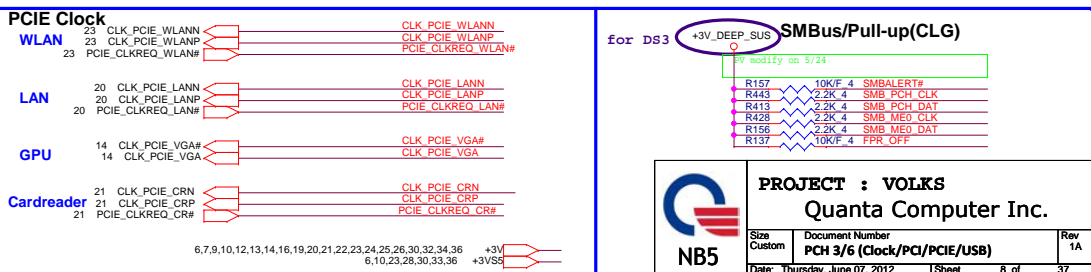
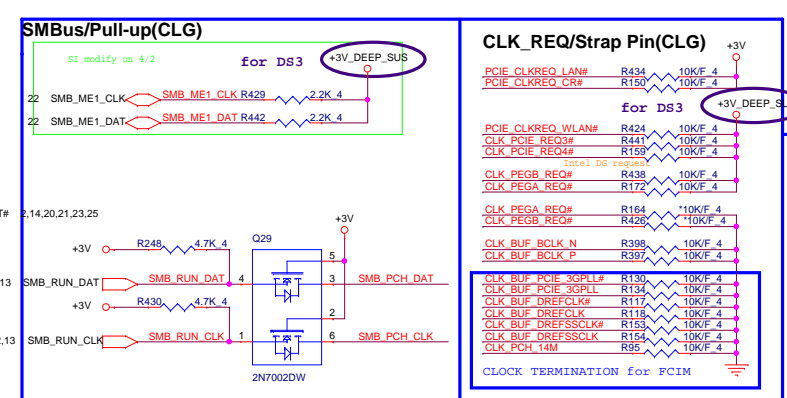
Vender	Size	P/N
EON	4MB	AKE39ZN0Q02 (EN25Q32B-104HIP)
MX	4MB	AKE39FP0Z02 (MX25L3206EM2I-12G)
AMIC	4MB	AKE39F-0800 (A25LQ32AM-F/Q)
Socket		DFHS08FS023



	PROJECT : VOLKS Quanta Computer Inc.		
	Size Custom	Document Number PCH 2/6 (HDA/RTC/SATA/SPI)	Rev. 1.
	Date: Thursday, June 07, 2012	Sheet 7 of 37	

PCH Strap Table

Pin Name	Strap description	Sampled	Configuration	Circuit						
SPKR	No reboot mode setting	PWROK	0 = Default (weak pull-down 20K) 1 = Setting to No-Reboot mode							
GNT3# / GPIO55	Top-Block Swap Override	PWROK	0 = "top-block swap" mode 1 = Default (weak pull-up 20K)							
INTVRMEN	Integrated 1.05V VRM enable	ALWAYS	Should be always pull-up							
HDA_DOCK_EN#/GPIO33	Flash Descriptor Security Only for Interposer	PWROK	0 = Override 1 = Default (weak pull-up 20K)							
GNT1# / GPIO51	Boot BIOS Selection 1 [bit-1]	PWROK	<table border="1"><thead><tr><th>GNT1#</th><th>GNT0#</th><th>Boot Location</th></tr></thead><tbody><tr><td>0</td><td>0</td><td>SPI LPC</td></tr></tbody></table>	GNT1#	GNT0#	Boot Location	0	0	SPI LPC	
GNT1#	GNT0#	Boot Location								
0	0	SPI LPC								
GPIO19 <i>Different from Calpella</i>	Boot BIOS Selection 0 [bit-0]	PWROK								
GNT2# / GPIO53	ESI strap (Server only)	PWROK	Should not be pull-down (weak pull-up 20K)	USE GPIO PIN						
NV_ALE	Intel Anti-Theft HDD protection Only for Interposer	PWROK	0 = Disable (Internal pull-down 20kohm)							
NV_CLE	DMI Termination voltage	PWROK	weak pull-down 20kohm							
HDA_SYNC	On-Die PLL VR Voltage Select	RSMRST	0 = Support by 1.8V (weak pull-down) 1 = Support by 1.5V							
HDA_SDO	Flash Descriptor Security	PWROK	0 = Override 1 = Default (weak pull-up 20K)							
GPIO8	Integrated Clock Chip Enable	RSMRST#	Should be pull-down (weak pull-up 20K)							
GPIO28 <i>Different from Calpella</i>	On-die PLL Voltage Regulator	RSMRST#	0 = Disable 1 = Enable (Default)							
SPI_MOSI	iTPM function Disable	APWROK	0 = Default (weak pull-down 20K) 1 = Enable							




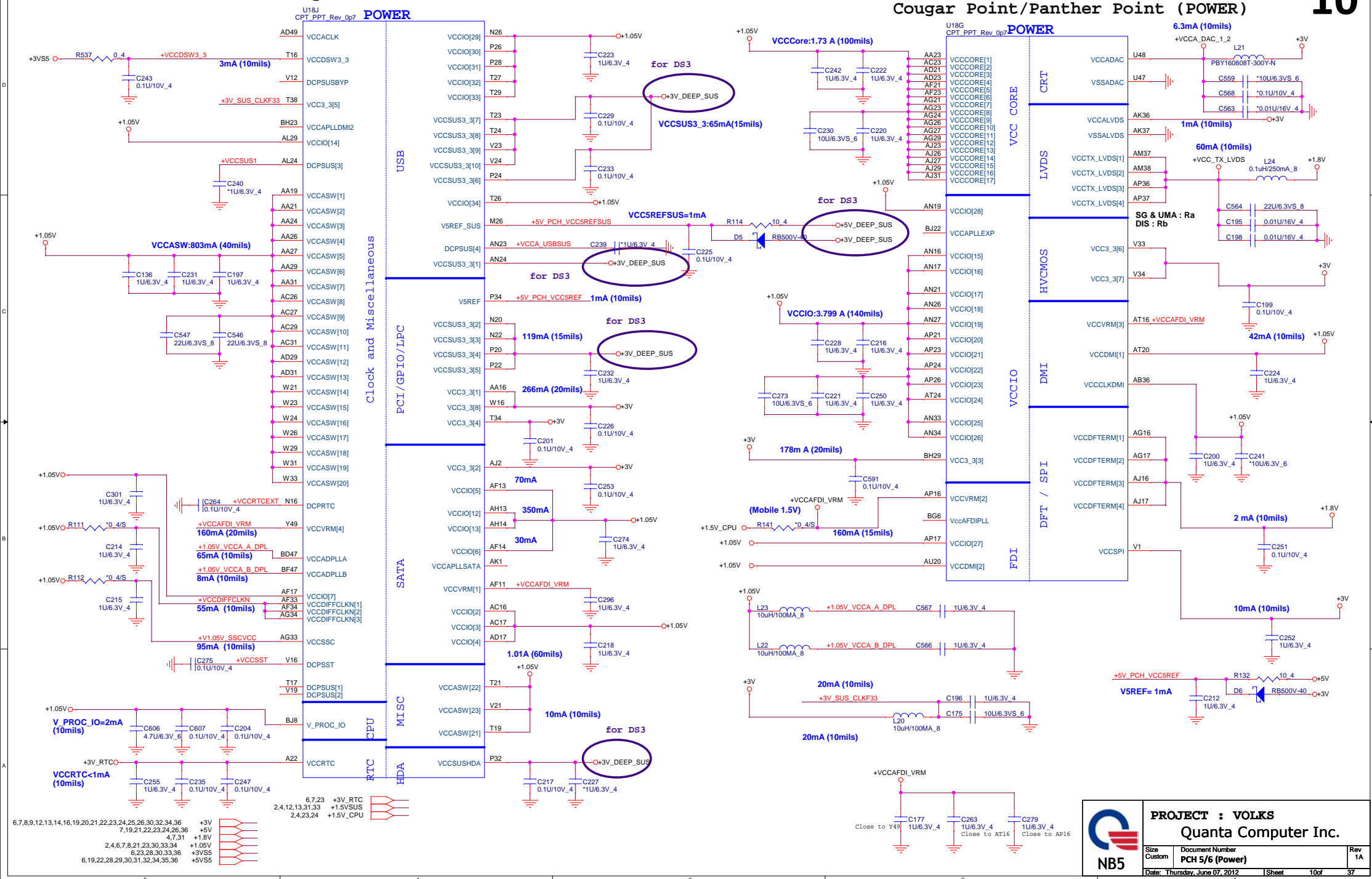


Model	BOARD_ID5	BOARD_ID4 14": 0 15": 1	BOARD_ID3 HM70: 0 HM77: 1	BOARD_ID2	BOARD_ID1 16": 0 26": 1	BOARD_ID0 UMA: 0 DIS: 1
U33 UMA	0	0	0	0	0	0
U33 DIS 128*16 VRAM	0	0	0	0	0	1
U33 DIS 256X16 VRAM	0	0	0	0	1	1
	0	0	0	1	1	1
U33 HM77	0	0	1	X	X	X
U33 HM70	0	0	0	X	X	X

The diagram shows the connection of the DS3 signal to the Rb and Ra ports of the SG and UMA blocks. The DS3 signal is provided by a 4-lane board (BOARD_ID0, BOARD_ID1, BOARD_ID2, BOARD_ID3) connected to the R147, R144, R166, R167, R138, R158, R355, R356, R78, R79, R84, R85, R423, and R422 pins. The Rb and Ra ports are connected to the SG and UMA blocks. The SG block has a Stuff input and an NC input. The UMA block has an Rb input and an Ra input. The Rb and Ra inputs are connected to the Rb and Ra ports of the SG and UMA blocks. The Rb and Ra ports are connected to the Rb and Ra inputs of the SG and UMA blocks. The Rb and Ra inputs are connected to the Rb and Ra ports of the SG and UMA blocks. The Rb and Ra ports are connected to the Rb and Ra inputs of the SG and UMA blocks.

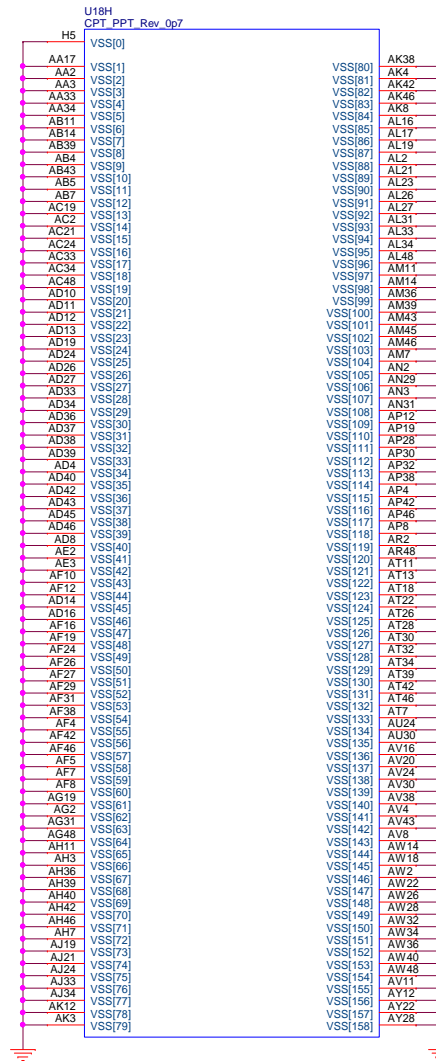
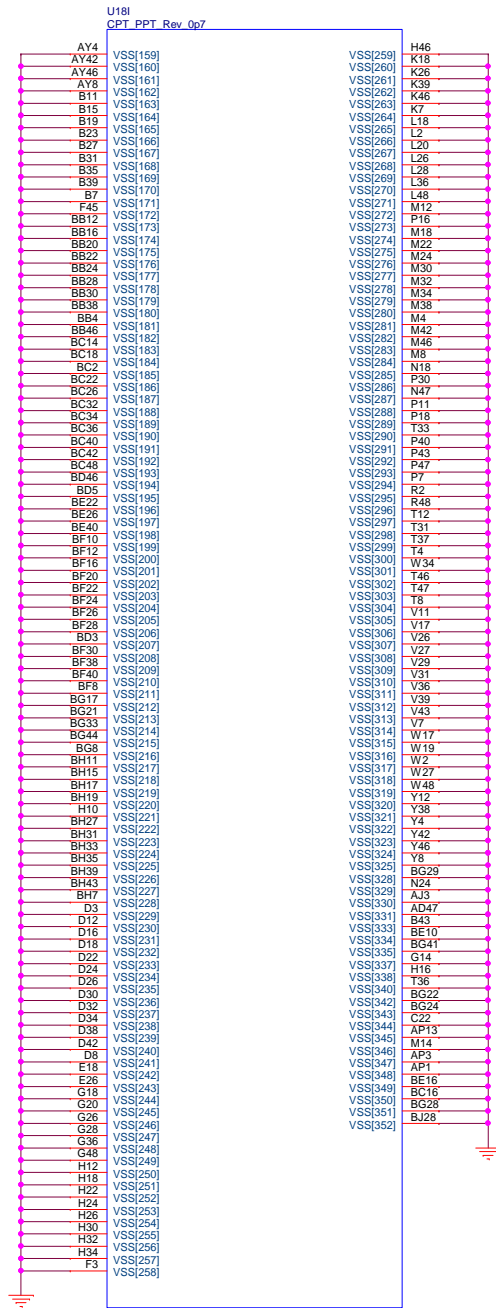
	SG	UMA
Stuff	Ra	Rb
NC	Rb	Ra


PROJECT : VOLKS
Quanta Computer Inc.
 Size Custom Document Number
 PCH 4/6 (GPIO) Rev 1A
 Date: Thursday, June 07, 2012 Sheet 9 of 37

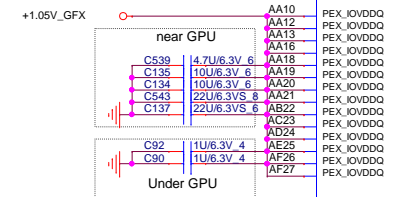


Cougar Point/Panther Point (GND)

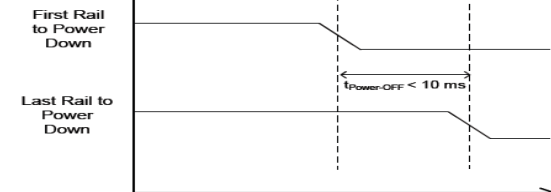
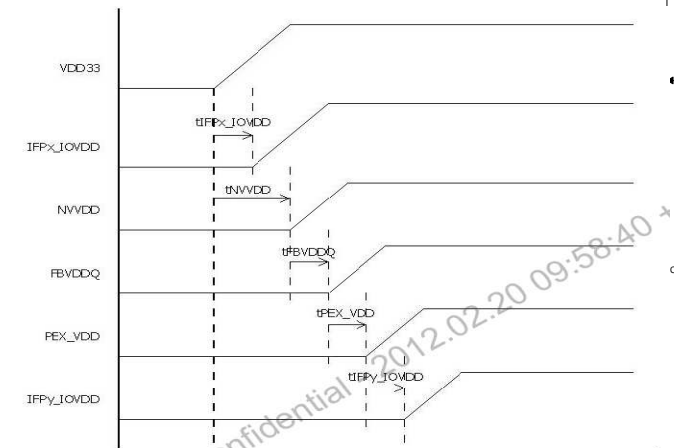
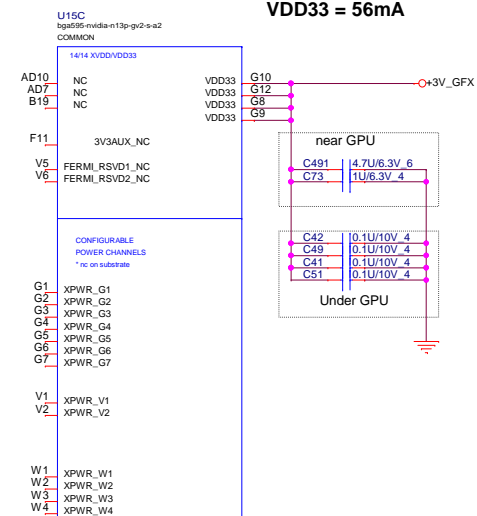
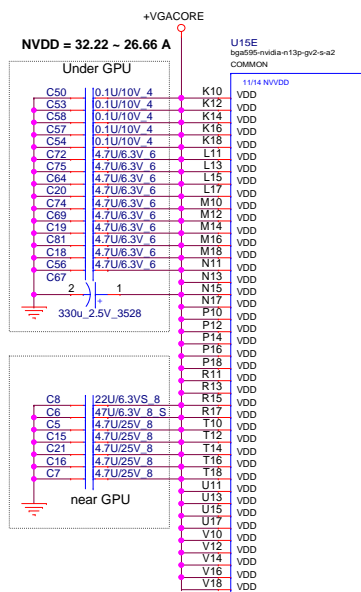
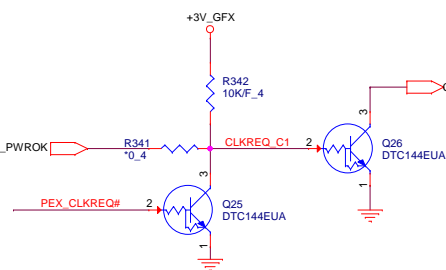
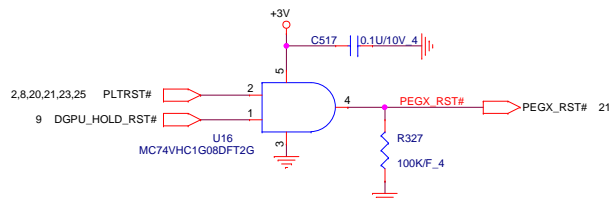
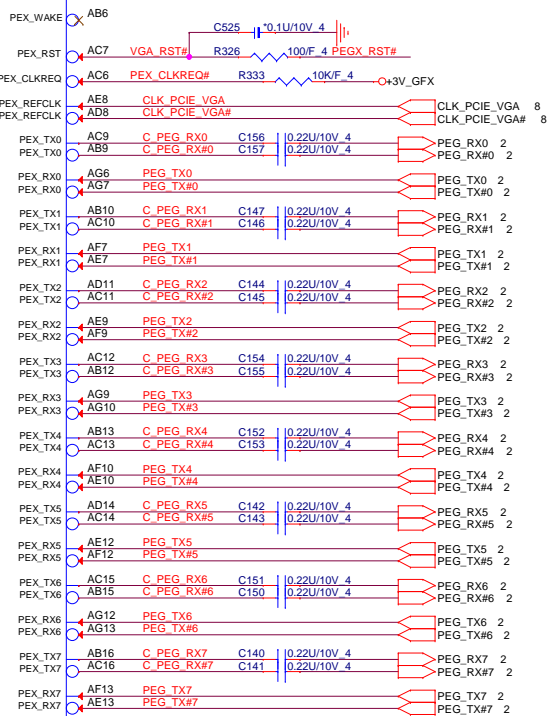
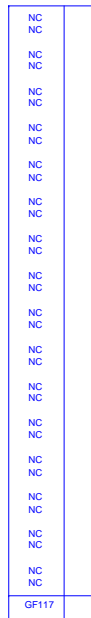
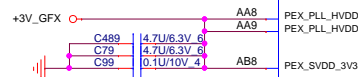
Cougar Point/Panther Point (GND)

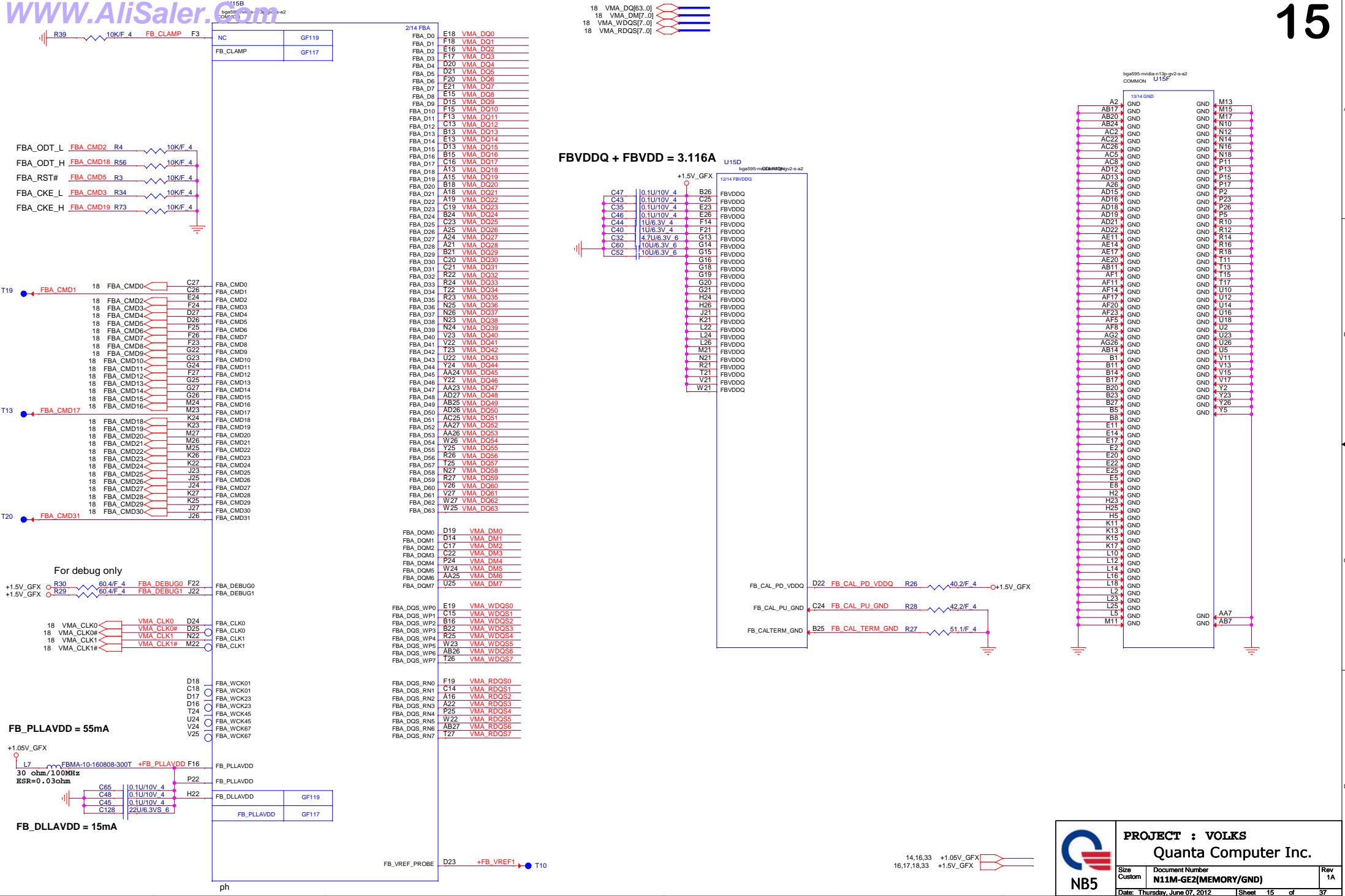




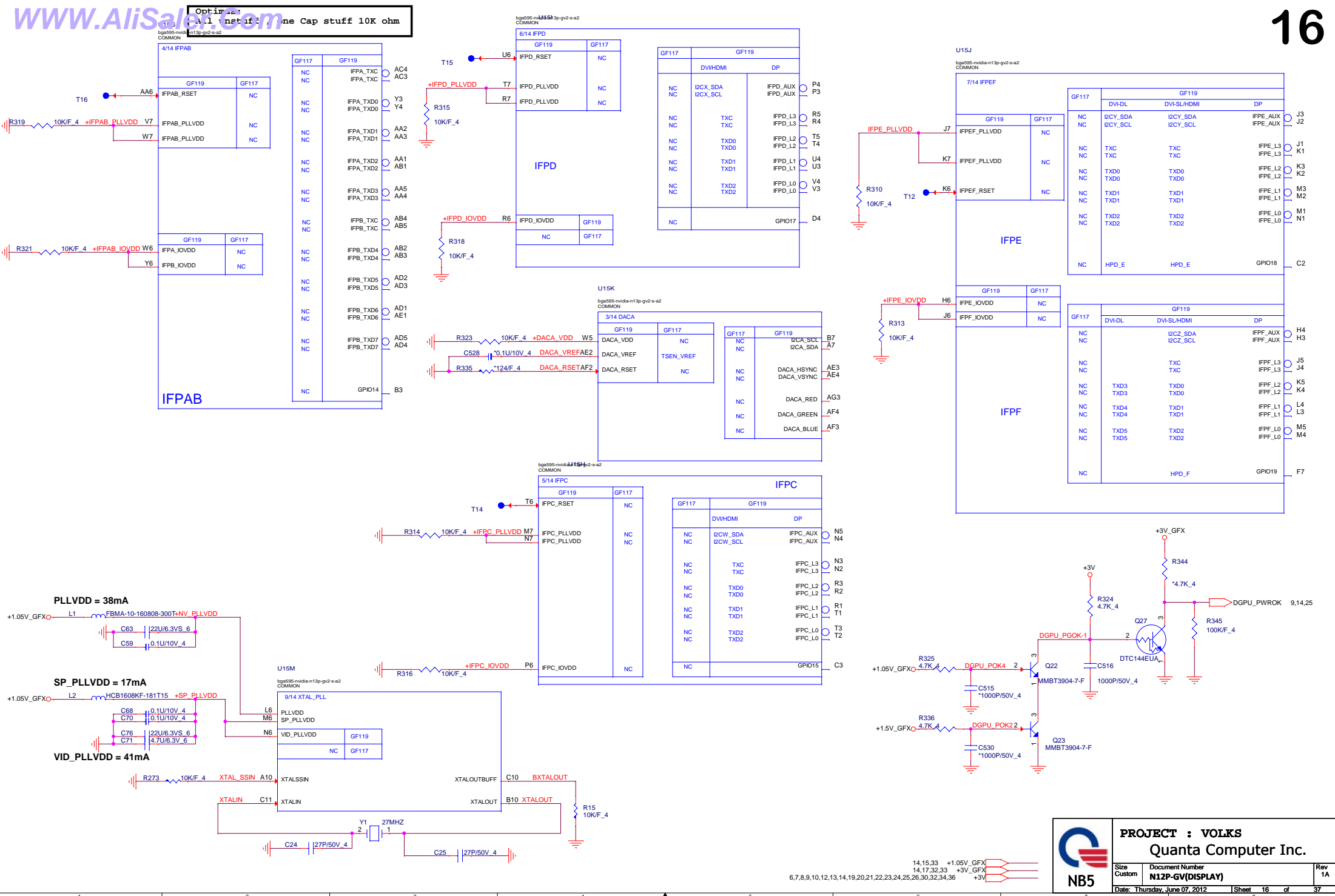


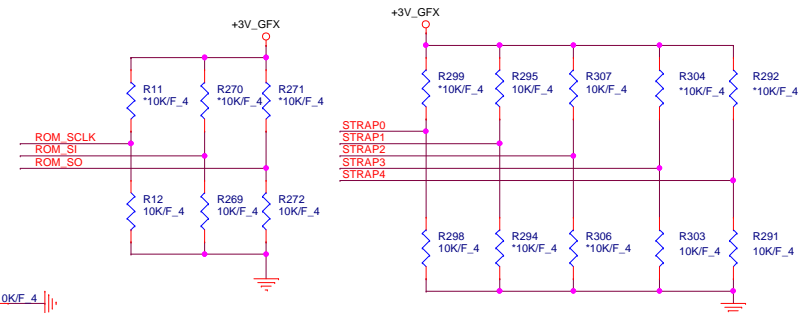
**PEX_PLL_HVDD +
PEX_SVDD 3V3 = 143mA**





Optimize the Cap stuff 10K ohm



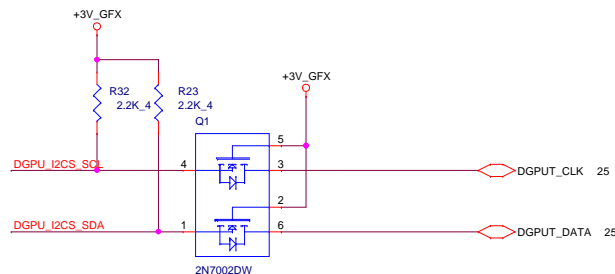
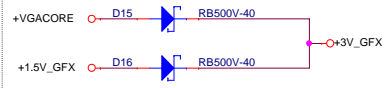


Binary Strap Mode Mapping

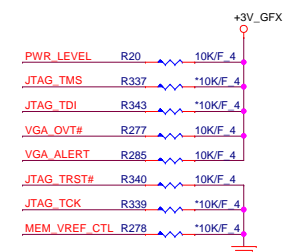
VRAM Configuration Table

RAMCFG [3:0]	DESCRIPTION	Vendor	Vendor P/N	QBCON P/N	HP P/N
	(MP)	Reserved			
0011	DDR3 256Mx16x4, 64bit, 2Gb,900MHz	Hynix	H5TQ4G63MFR-11C	AKD5PGWTW00	AKD5PGWTW01
0101	DDR3 256Mx16x4, 64bit, 2Gb,900MHz	Micron	MT41K256M16HA-10TG:E	AKD5PGSTL01	AKD5PGSTL02
1100	DDR3 128Mx16x4, 64bit, 1Gb,900MHz	Hynix	H5TQ2G63DFR-11C	AKD5MGWTW12	AKD5MGWTW13
0101	DDR3 128Mx16x4, 64bit, 1Gb,900MHz	Samsung	K4W2G1646C-HC11	AKD5MGWT513	AKD5MGWT508
	(OOC)				
0001	DDR3 256Mx16x4, 64bit, 2Gb,900MHz	Samsung	K4W4G1646B-HC11	AKD5MGWT518	AKD5MGWT517
0100	DDR3 256Mx16x4, 64bit, 2Gb,900MHz	Hynix	H5TQ4G63AFR-11C	AKD5MGWT519	AKD5MGWT518
1011	DDR3 128Mx16x4, 64bit, 1Gb,900MHz	Samsung	K4W2G1646B-HC11	AKD5MGGT521	AKD5MGGT522

25 GB2-64 and GB4-128 GPIO Desdription



GPIO pin Name	Normal Function	I/O	Functional Description	Recommended Default Pull-up or Pull-down
GPIO0	GPU_VID4	O	GPU Core VDD VID4	Strap to boot NVVDD
GPIO1	GPU_VID3	O	GPU Core VDD VID3	Strap to boot NVVDD
GPIO2	LCD_BL_PWM	O	Panel Backlight PWM Brightness Control	100 K pull-down
GPIO3	LCD_VCC or PSI	O	Panel Power Enable or Phase Shedding	LCD_VCC: 100k pull-down PSI: 10k pull-up or pull-down; stuff as needed to disable phase shedding by default
GPIO4	LCD_BLEN	O	Panel Backlight Enable	100 K pull-down
GPIO5	GPU_VID1	O	GPU Core VDD VID1	Strap to boot NVVDD
GPIO6	GPU_VID2	O	GPU Core VDD VID2	Strap to boot NVVDD
GPIO7	3D Vision	O	3D Vision Left/Right signal	100 K pull-down
GPIO8	OVERT	I/O	Active Low Thermal Catastrophic Over Temperature	100 K pull-up
GPIO9	ALERT	I/O	Active Low Thermal Alert	100 K pull-up
GPIO10	MEM_VREF_CTL	O	Memory VREF Control	100 K pull-down
GPIO11	GPU_VID0	O	GPU Core VDD VID0	Strap to boot NVVDD
GPIO12	PWR_LEVEL	I	AC power detect or power supply overdraw input	100 K pull-up
GPIO13	GPU_VID5	O	GPU Core VDD VID5	Strap to boot NVVDD
GPIO14	HPD_AB	I	Hot Plug Detect for IFPAB	See Figure 76
GPIO15	HPD_C	I	Hot Plug Detect for IFFC	See Figure 76
GPIO16	PSI or MEM_VDD0_CTL	O	Phase Shedding or Memory VDD VID	PSI: 10k pull-up or pull-down; stuff as needed to disable phase shedding by default MEM_VDD0_CTL: Strap to boot FBVDD/Q
GPIO17	HPD_D	I	Hot Plug Detect for IFPD	See Figure 76
GPIO18	HPD_E	I	Hot Plug Detect for IFPE	See Figure 76
GPIO19	HPD_F	I	Hot Plug Detect for IFFP	See Figure 76
GPIO20	Reserved			
GPIO21	Reserved			

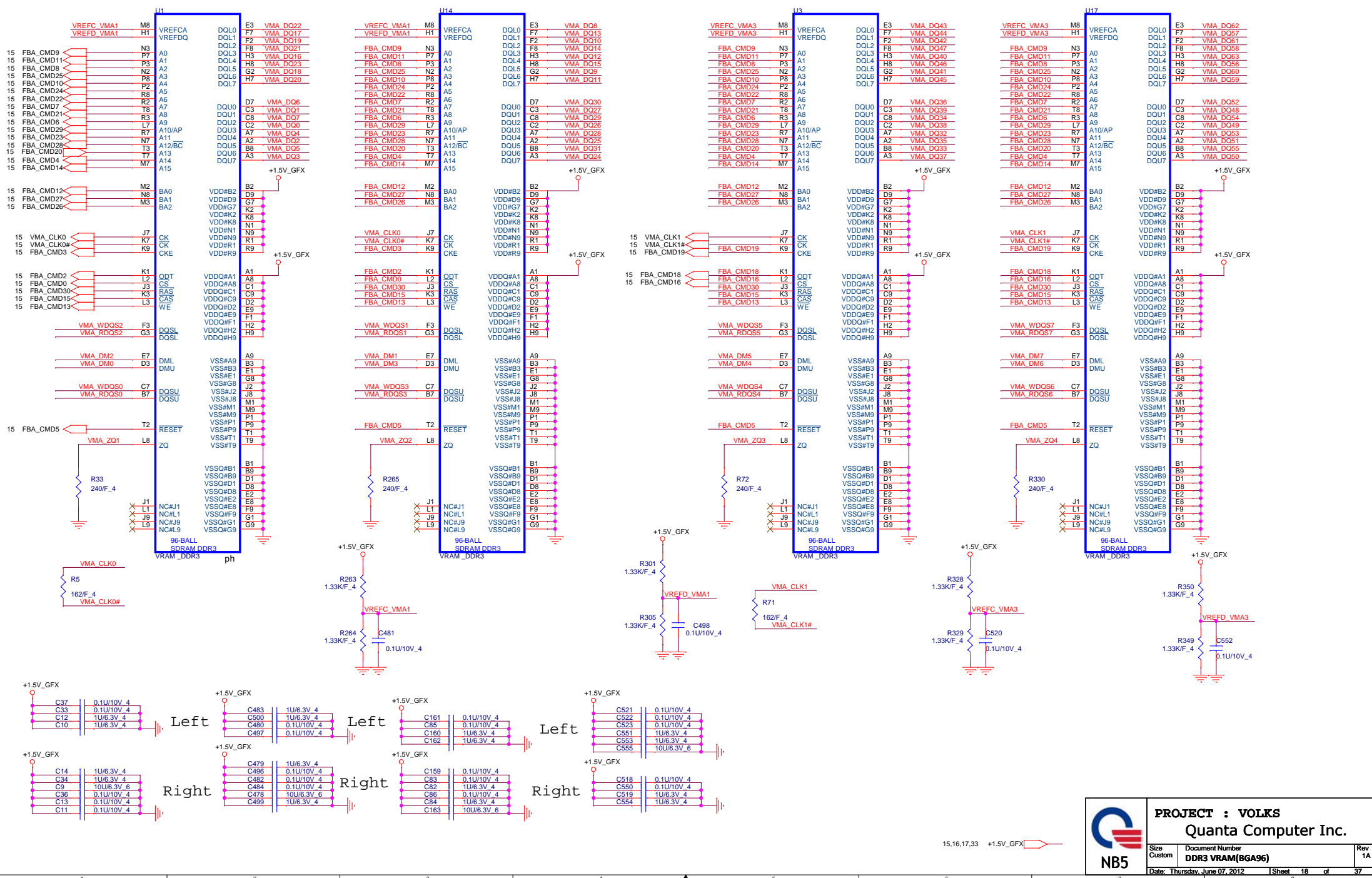


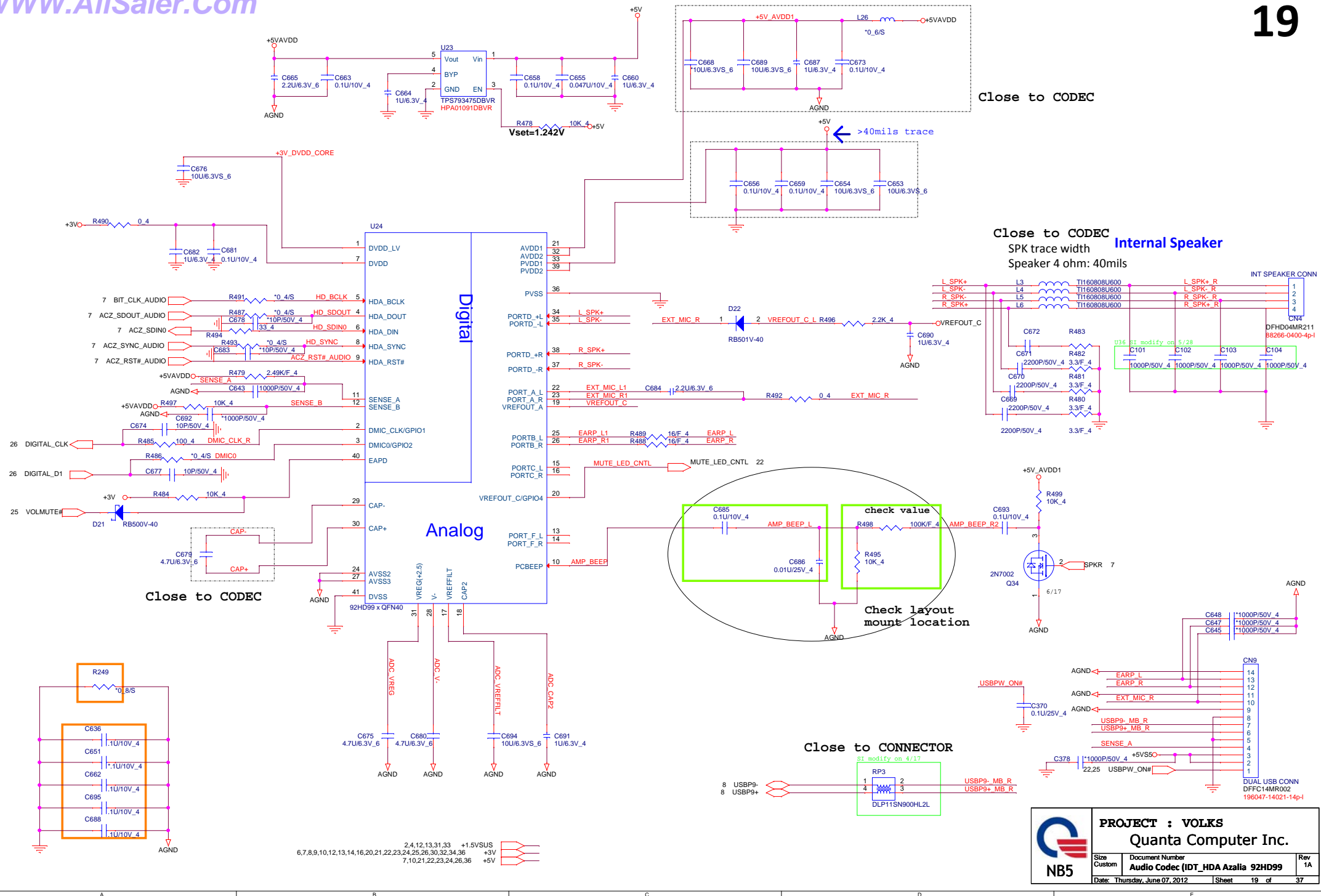
14,16,32,33	+3V_GFX
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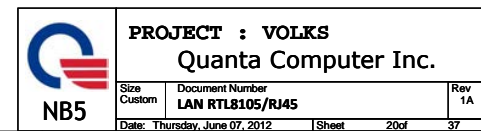


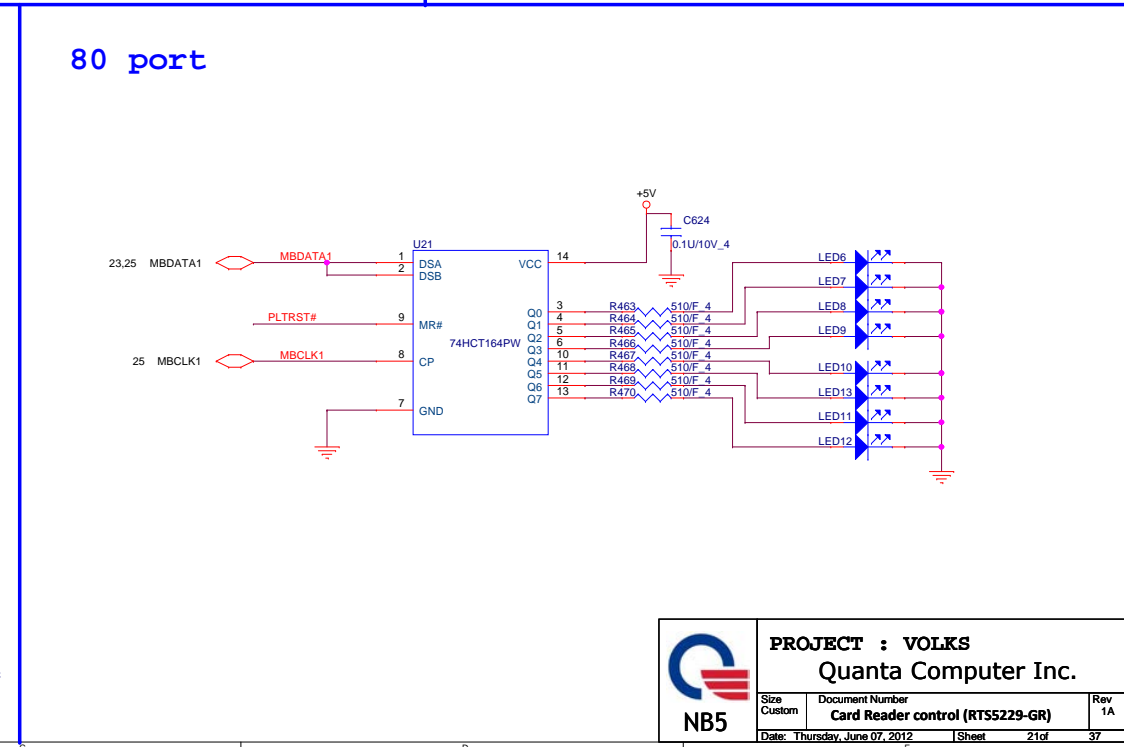
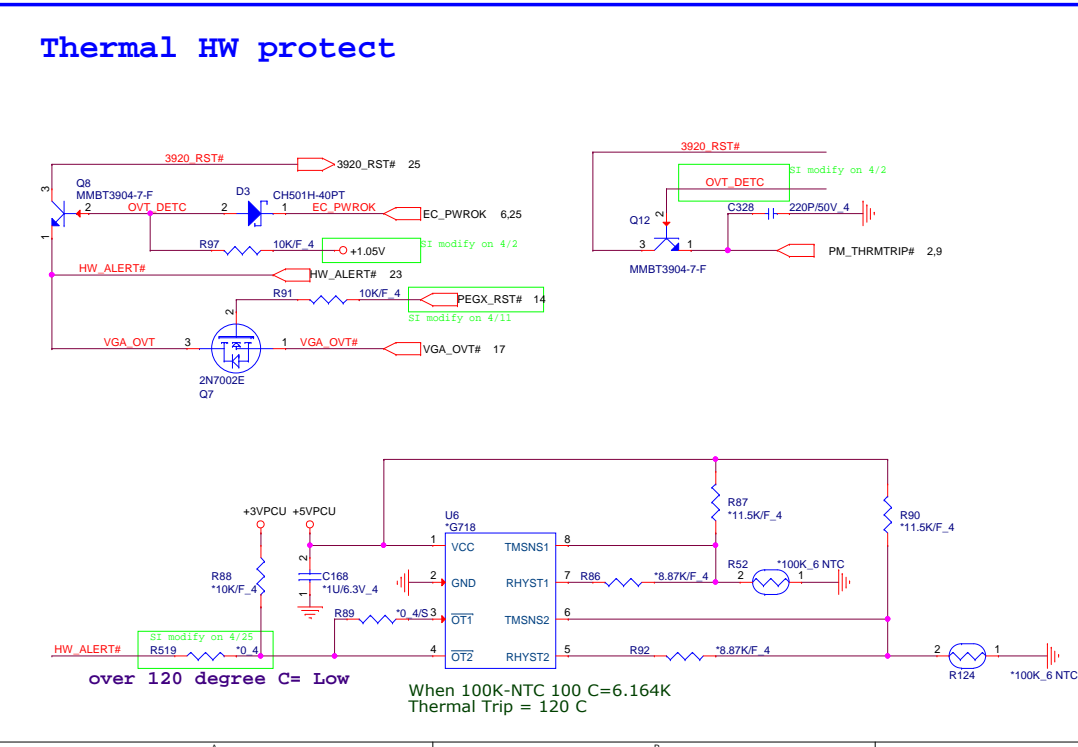
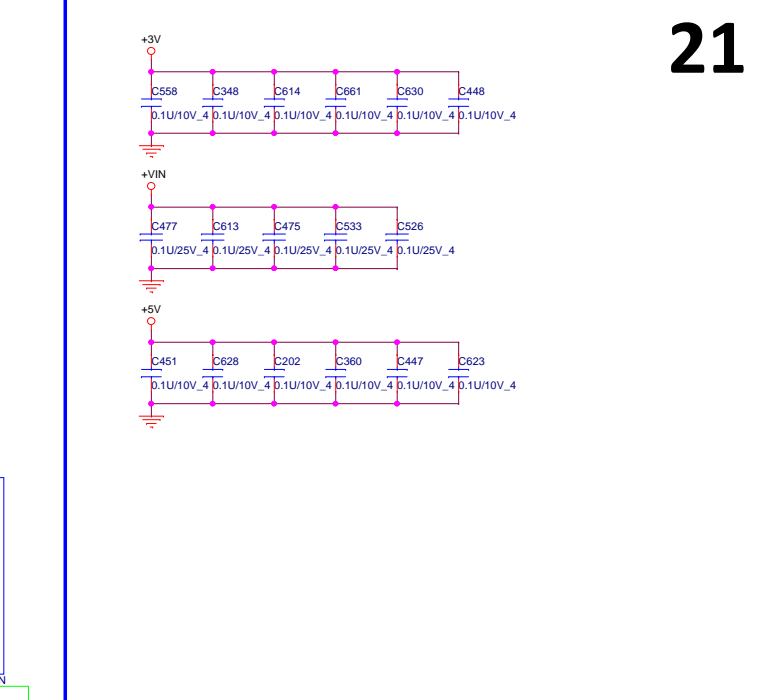
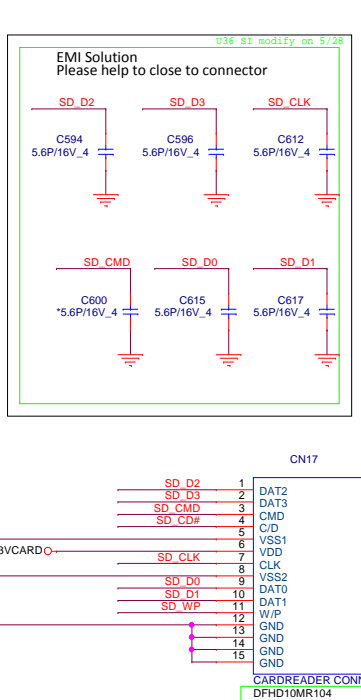
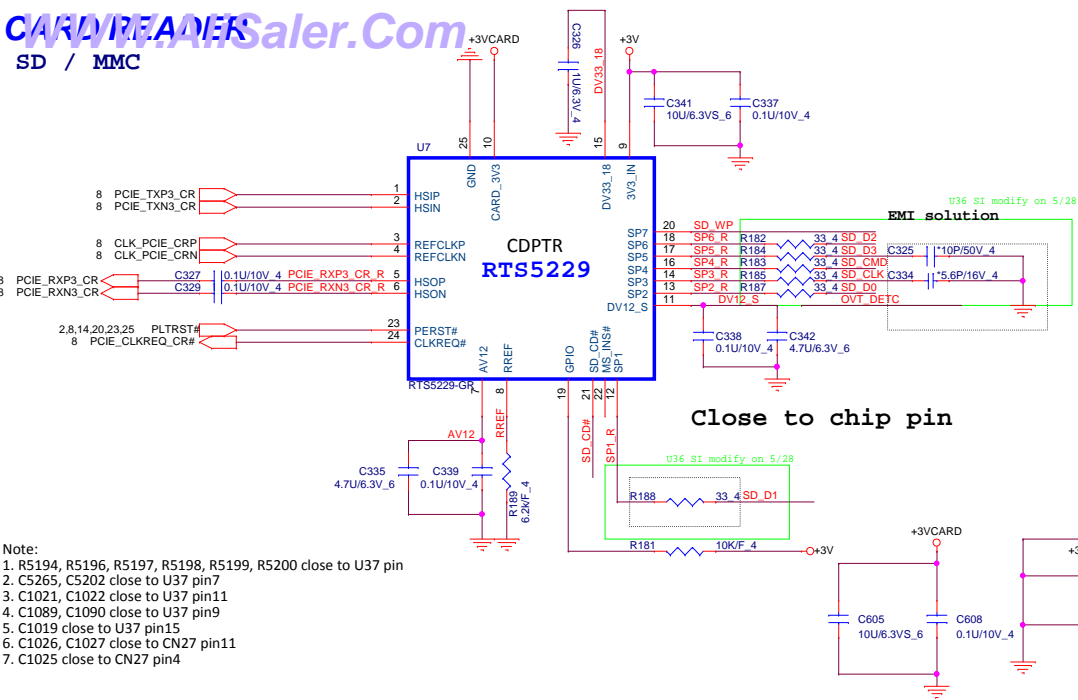
Size Custom	Document Number N12P-GV(GPIO/STRAPS)	Rev 1A
Date: Thursday, June 07, 2012	Sheet 17 of 37	

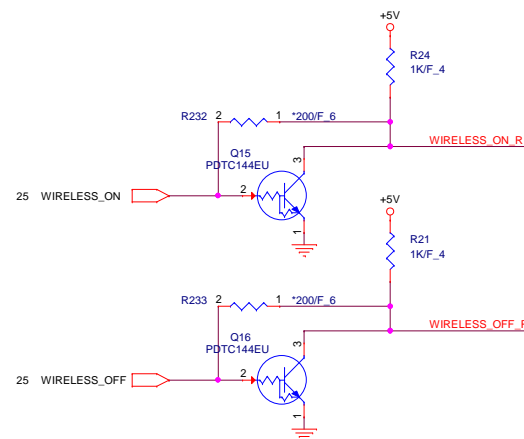
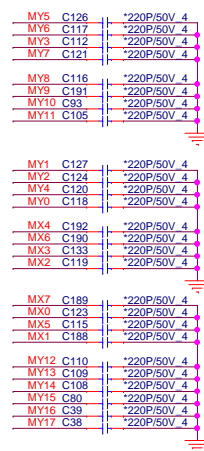
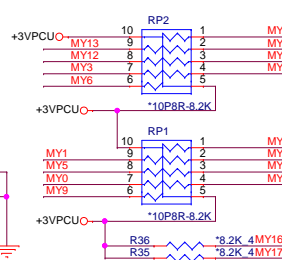
15 VMA_DQ[63:0]
15 VMA_DM[7:0]
15 VMA_WDQS[7:0]



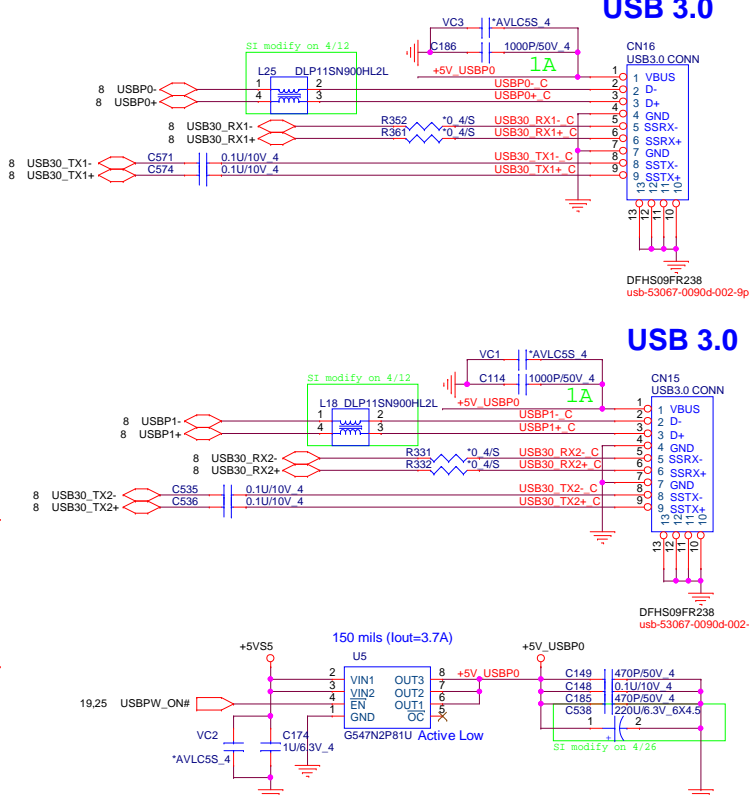
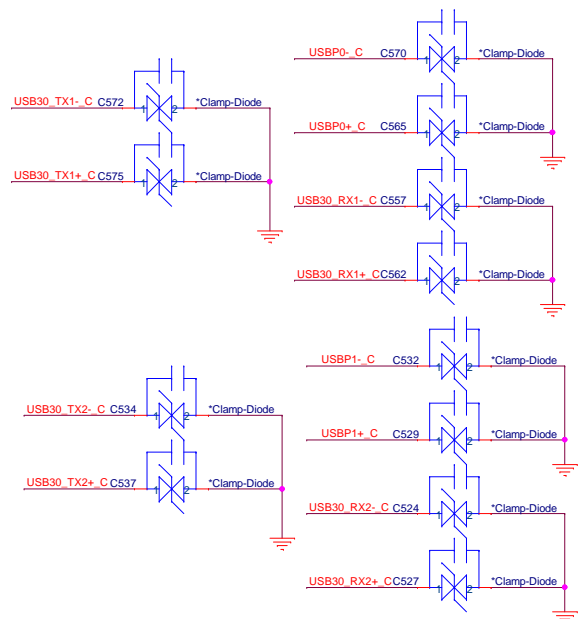




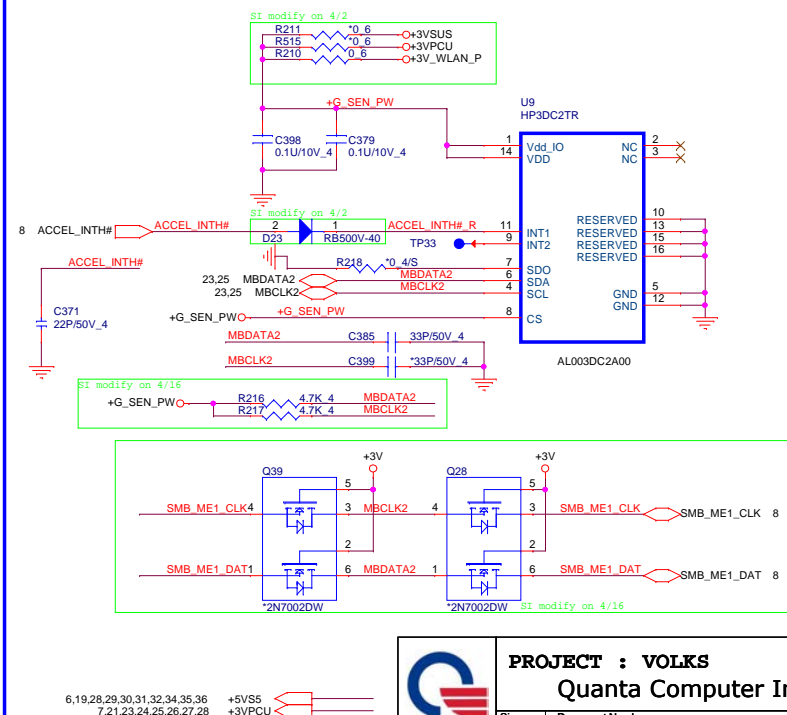


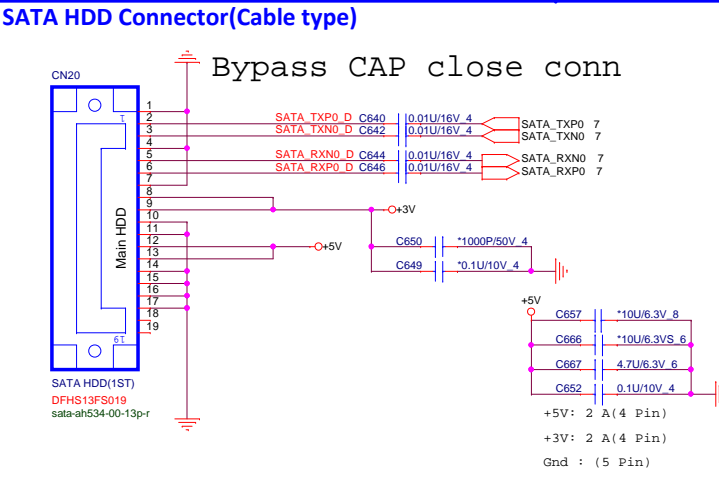
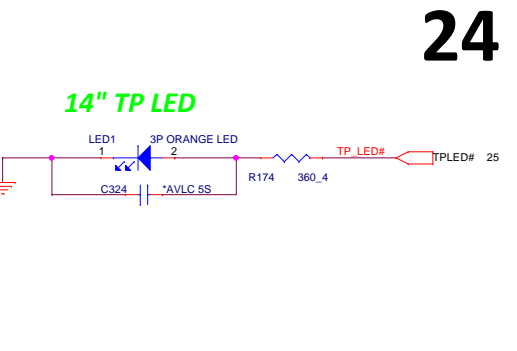
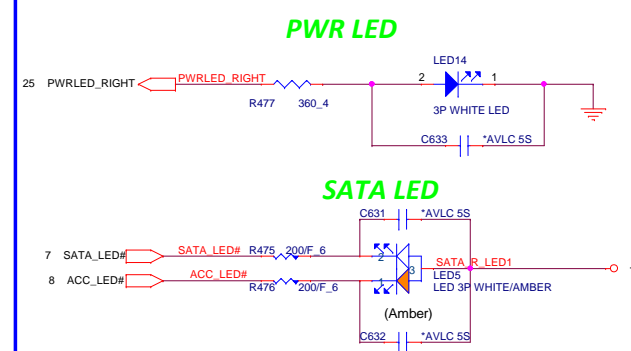
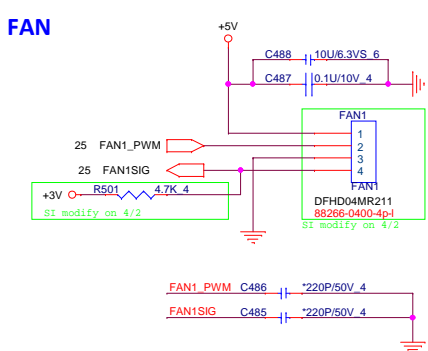
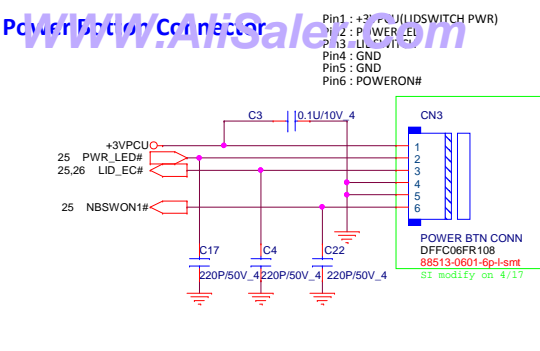


USB 3.0

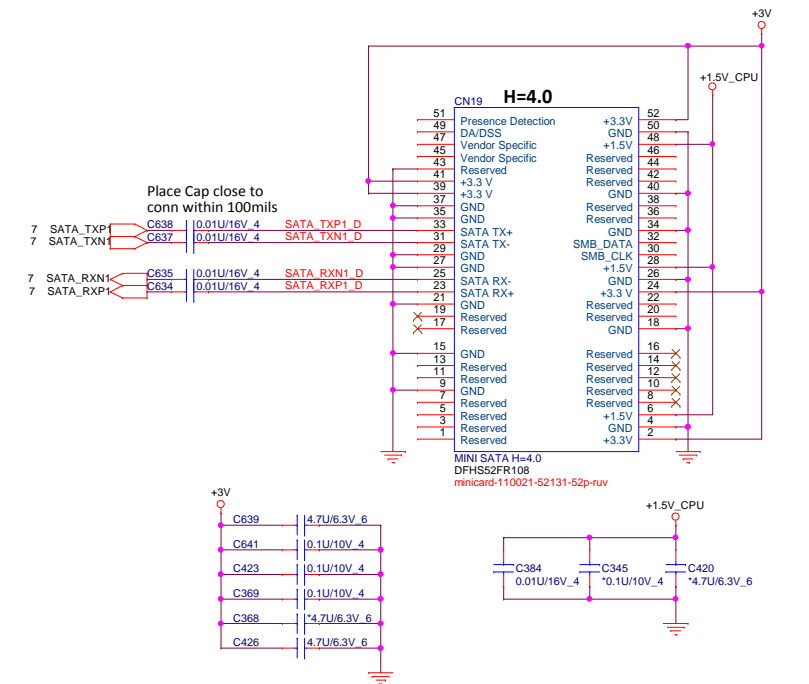


Accelerometer Sensor

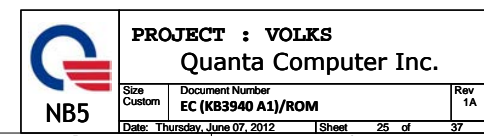


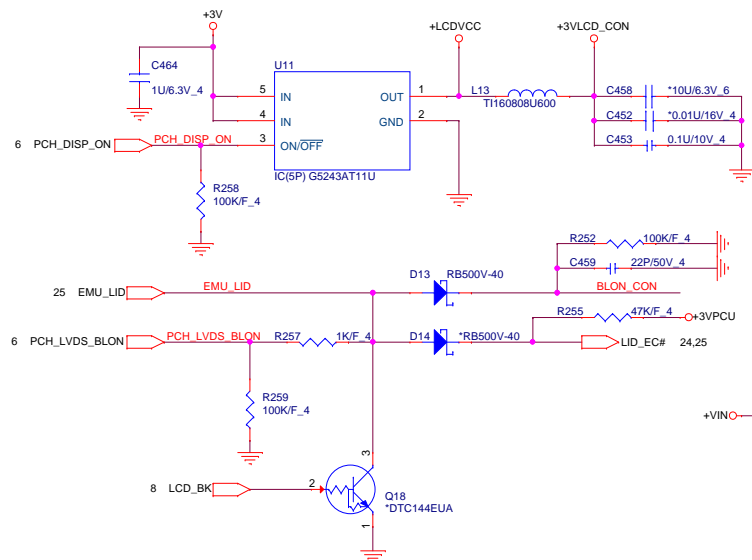
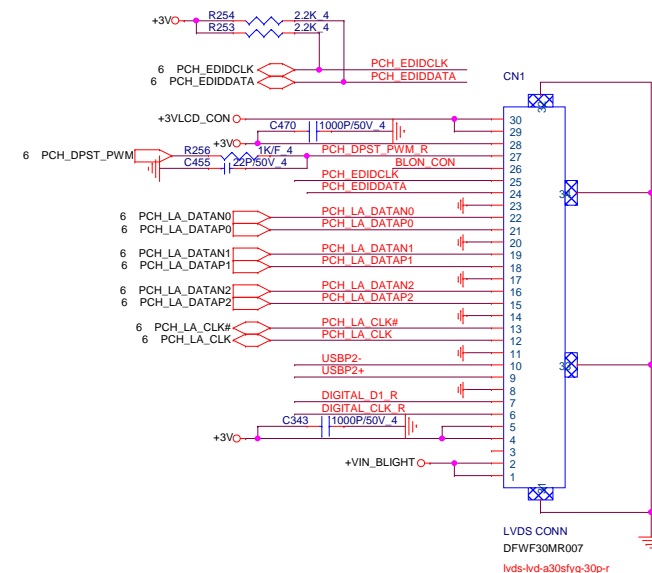
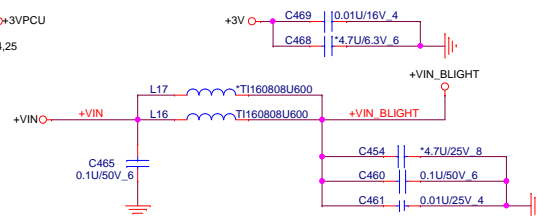
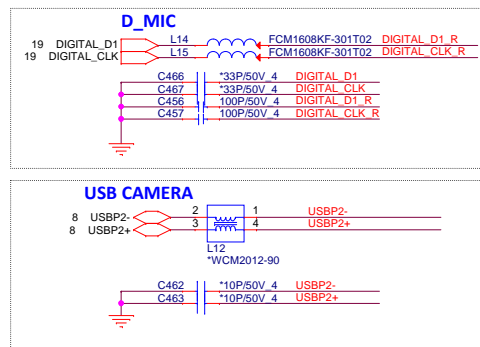


Mini PCI-E Card 2- Full size mSATA



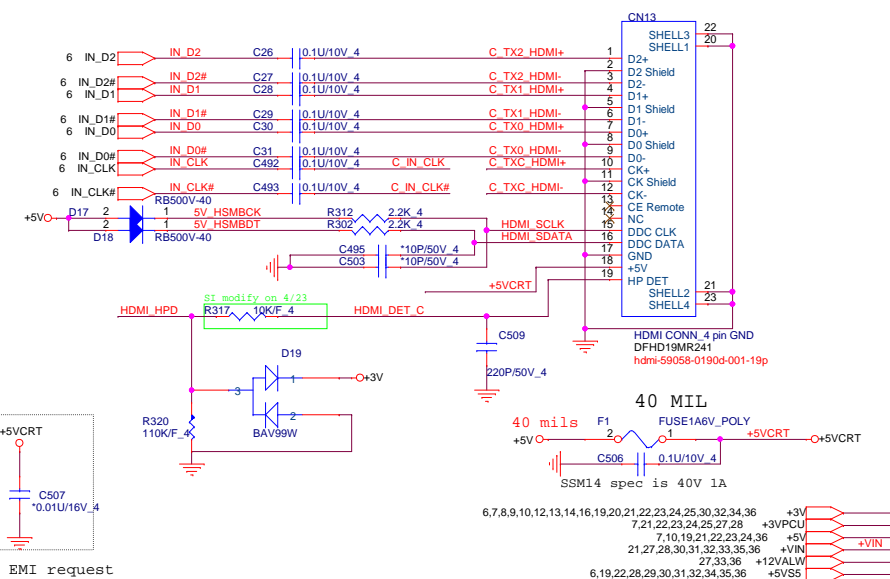
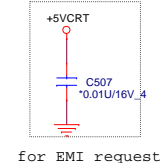
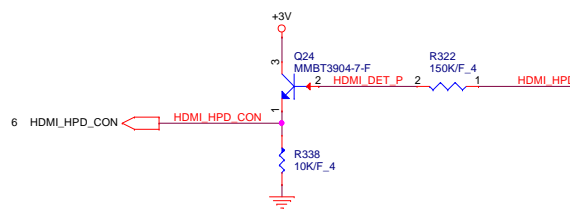
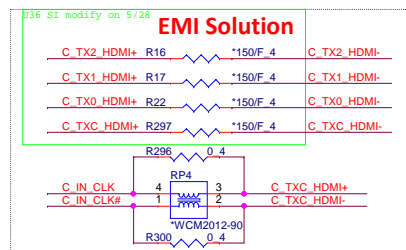
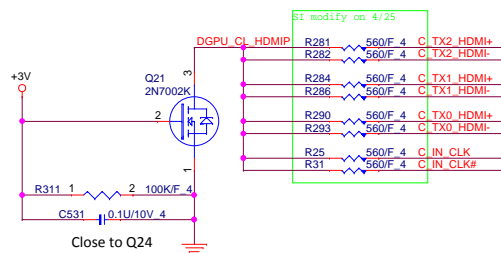
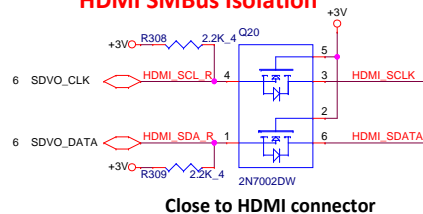
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Size Custom	Document Number	SATA HDD/ODD/MSATA CONN	
Date: Thursday, June 07, 2012	Sheet	24 of	37




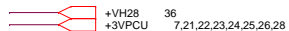


HDMI Conn.

HDMI SMBus Isolation



		PROJECT : VOLKS	
		Quanta Computer Inc.	
Size Custom	Document Number LCD Connector (LVDS)	Rev 1A	
Date: Thursday, June 07, 2012	Sheet 26 of 37		



+5V +/- 5%
Countinue current:4A
Peak current:6A
OCP minimum:7.5A

+3.3 Volt +/- 5%
Countinue current:4A
Peak current:6A
OCP minimum:7.5A

Current Limit setting
 $VILIMx = (RILIMx \times 10\mu A) / 10 = IILIMx \times RDS(ON)$
 $RILIMx = (IILIMx \times RDS(ON)) \times 10 / 10\mu A$

TONSEL= VREG5
 Vout1=400kHz/Vout2=500kHz

25,29,30,31 HWPG

+3VS5

21,26,27,30,31,32,33,35,36
 6,10,23,30,33,36
 6,19,22,29,30,31,32,34,35,36
 7,21,22,23,24,25,26,27

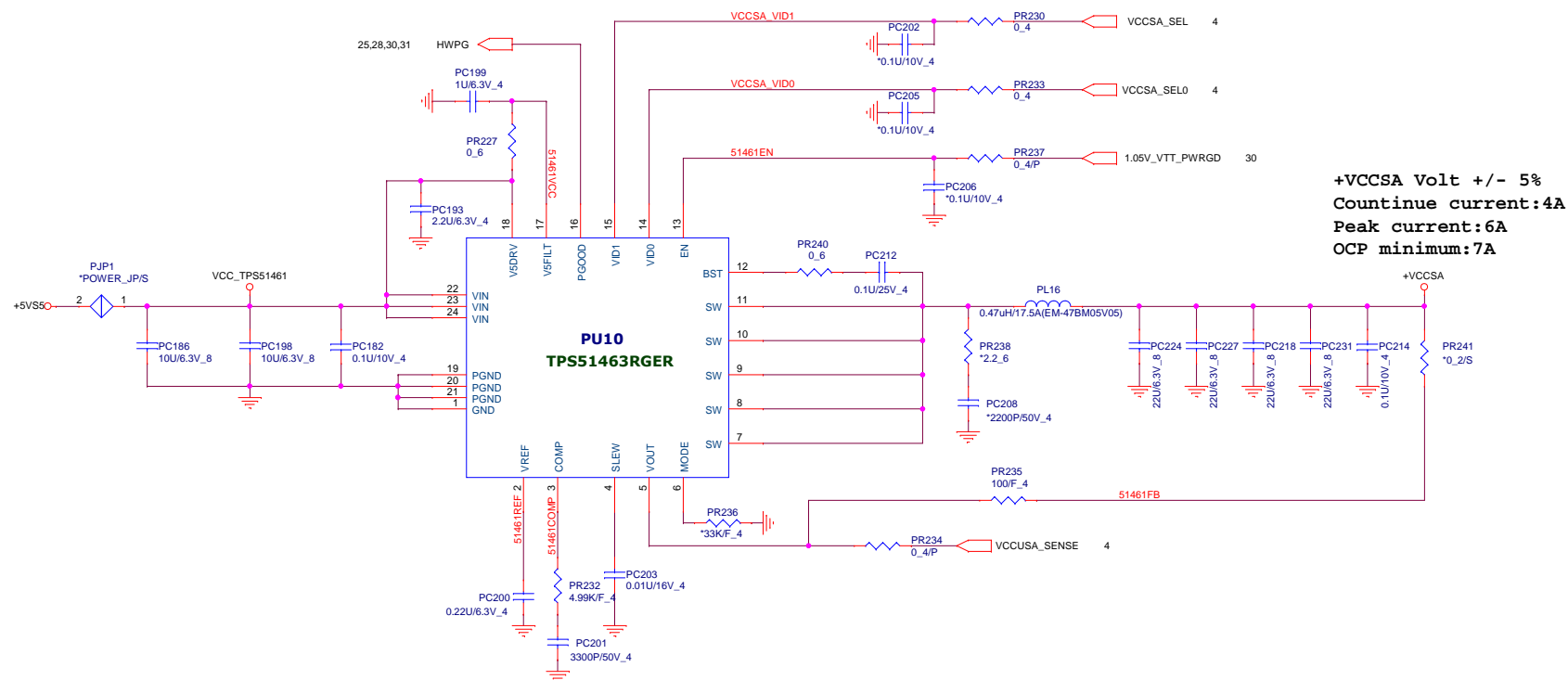
+VIN
 +3VS5
 +5VS5
 +3VPCU

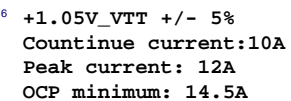
NB5	PROJECT :VOLKS		
	Quanta Computer Inc.		
	Size	Document Number	Rev
	Custom	3/5VS5 (RT8223P)	A
Date: Thursday, June 07, 2012			
Sheet 28 of 37			

TPS51463RGER/AL051463000
For CPU ULV system agent
voltage slew rate of 0.5 -10 mV/μs

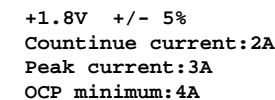
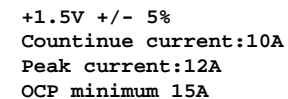
SEL0	SEL1	+VCCSA
0	0	0.9V
0	1	0.8V
1	0	0.725V
1	1	0.675V


SELO	SEL1	+VCCSA
0	0	0.9V
0	1	0.85V
1	0	0.775V
1	1	0.75V

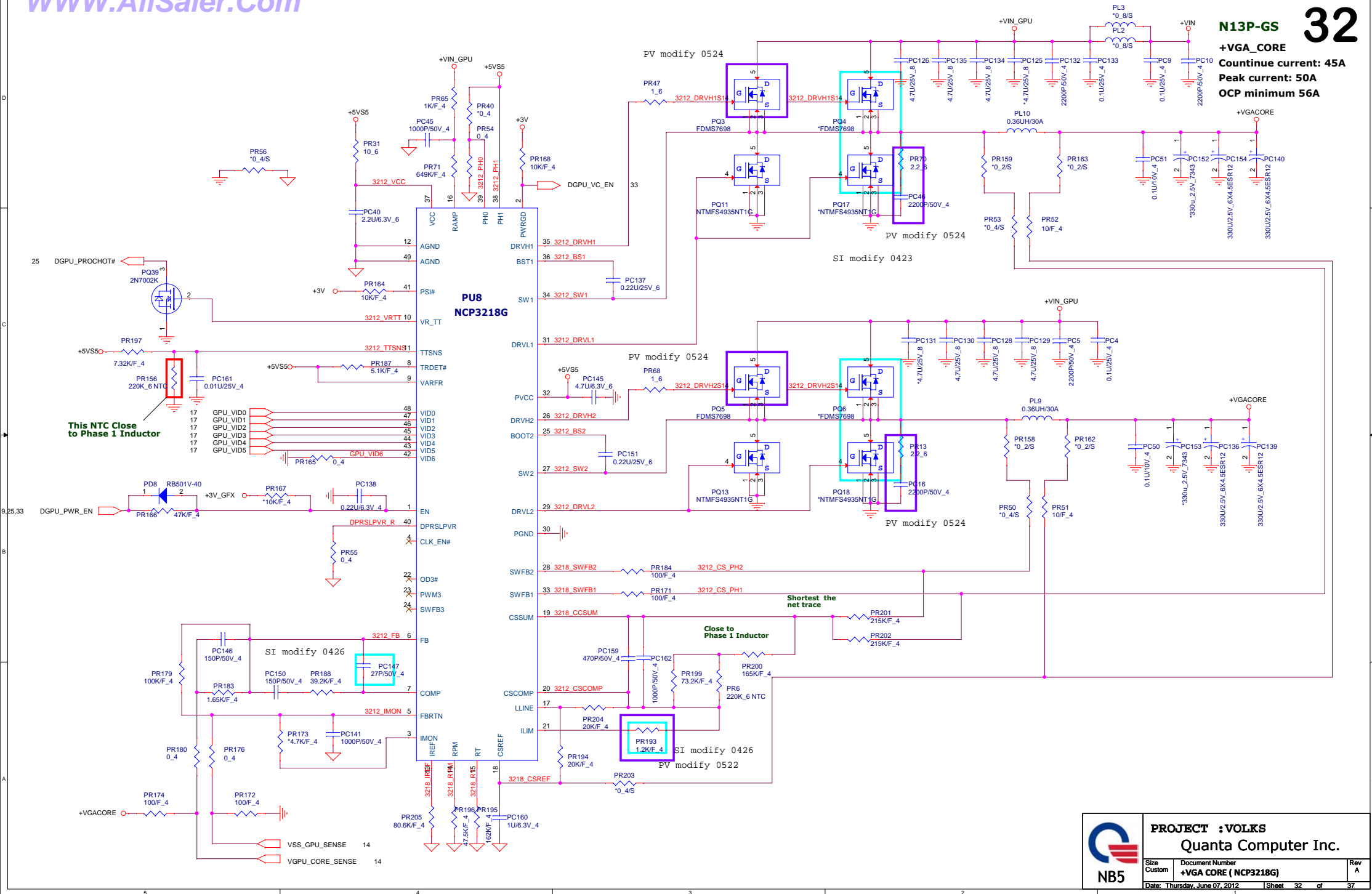




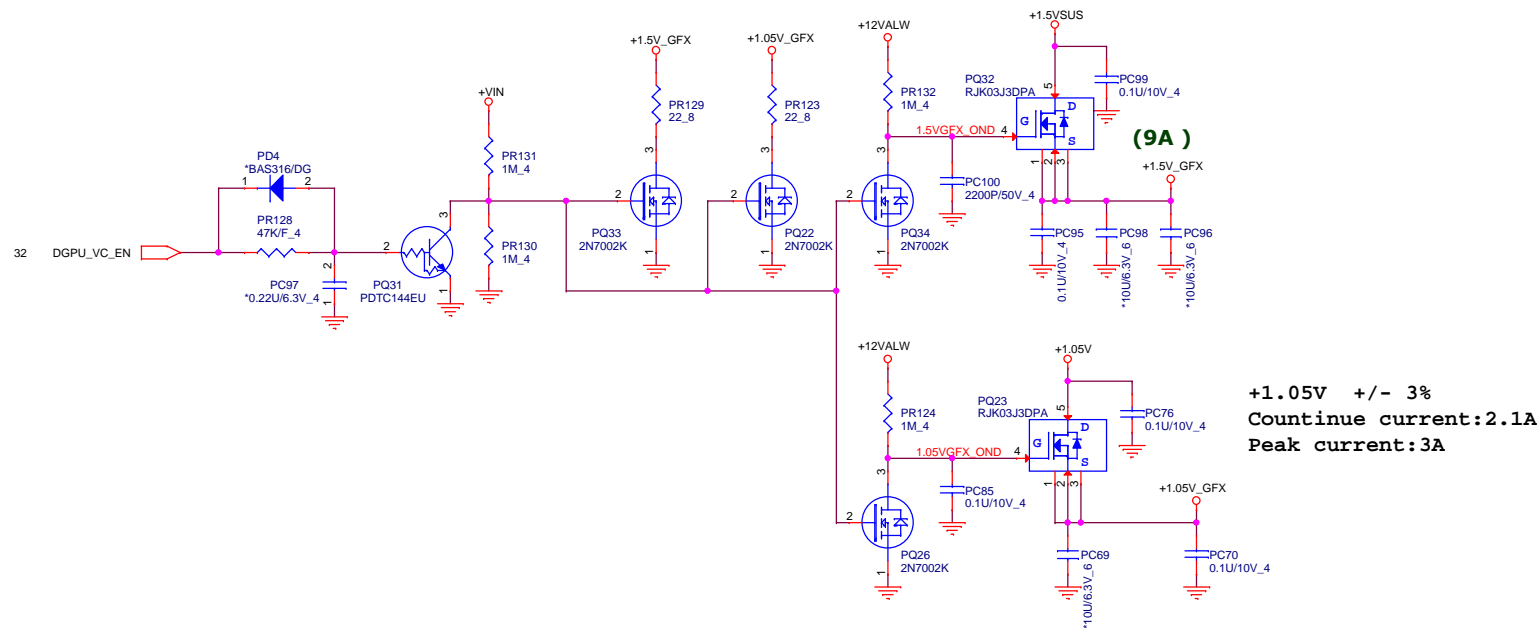
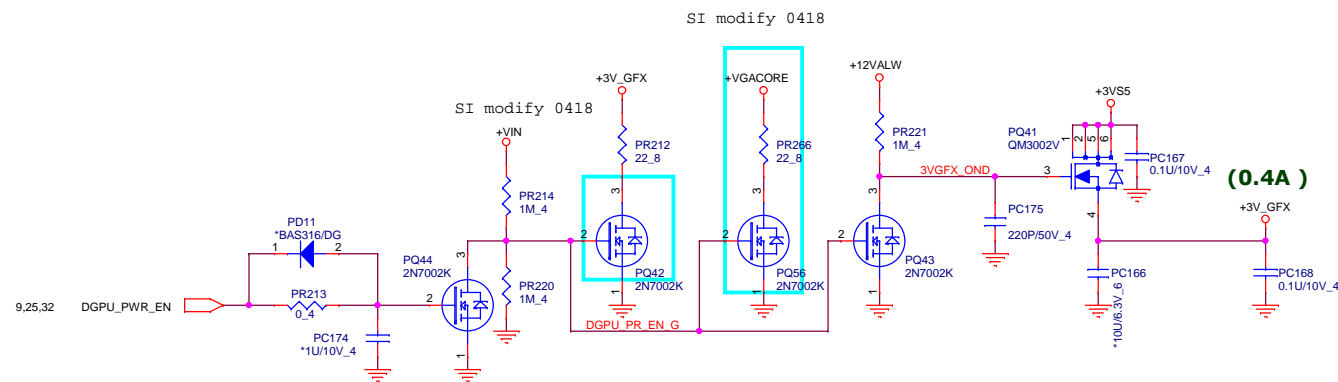
WWW.AliSaler.Com



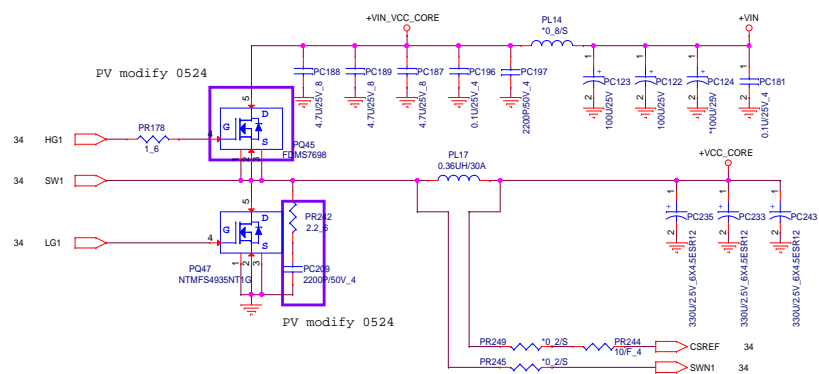
	PROJECT :VOLKS Quanta Computer Inc.		
	Size Custom	Document Number DDR3 (RT8207)	Rev A
	Date: Thursday, June 07, 2012	Sheet 31 of 37	



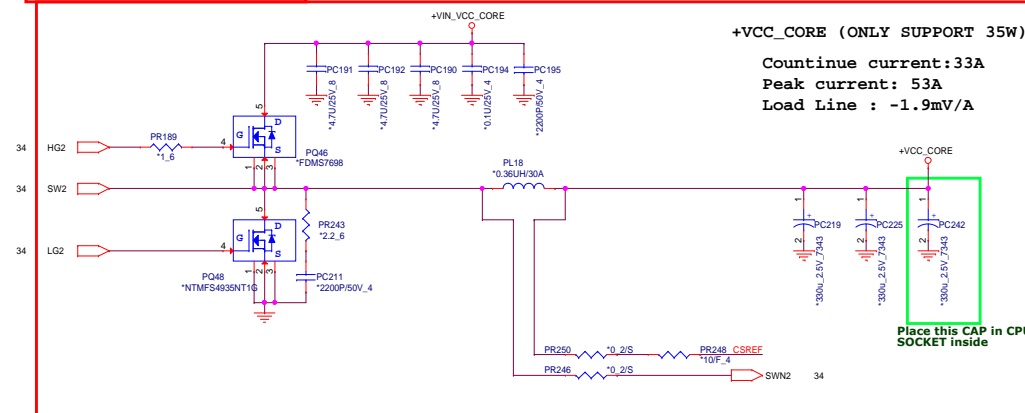
2,4,12,13,31 +1.5VSUS
6,10,23,28,30,36 +3VSS
14,16,17,32 +3V_GFX
15,16,17,18 +1.5V_GFX
14,15,16 +1.05V_GFX
27,36 +12VALW
2,4,6,7,8,10,21,23,30,34 +1.05V







Dummy This Schematic
For CPU 1-Phase operation

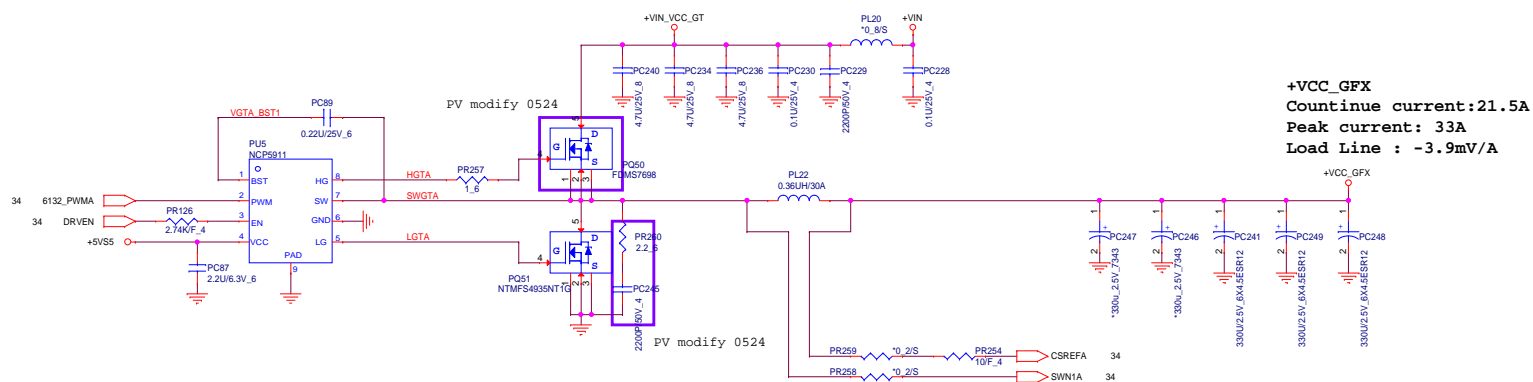


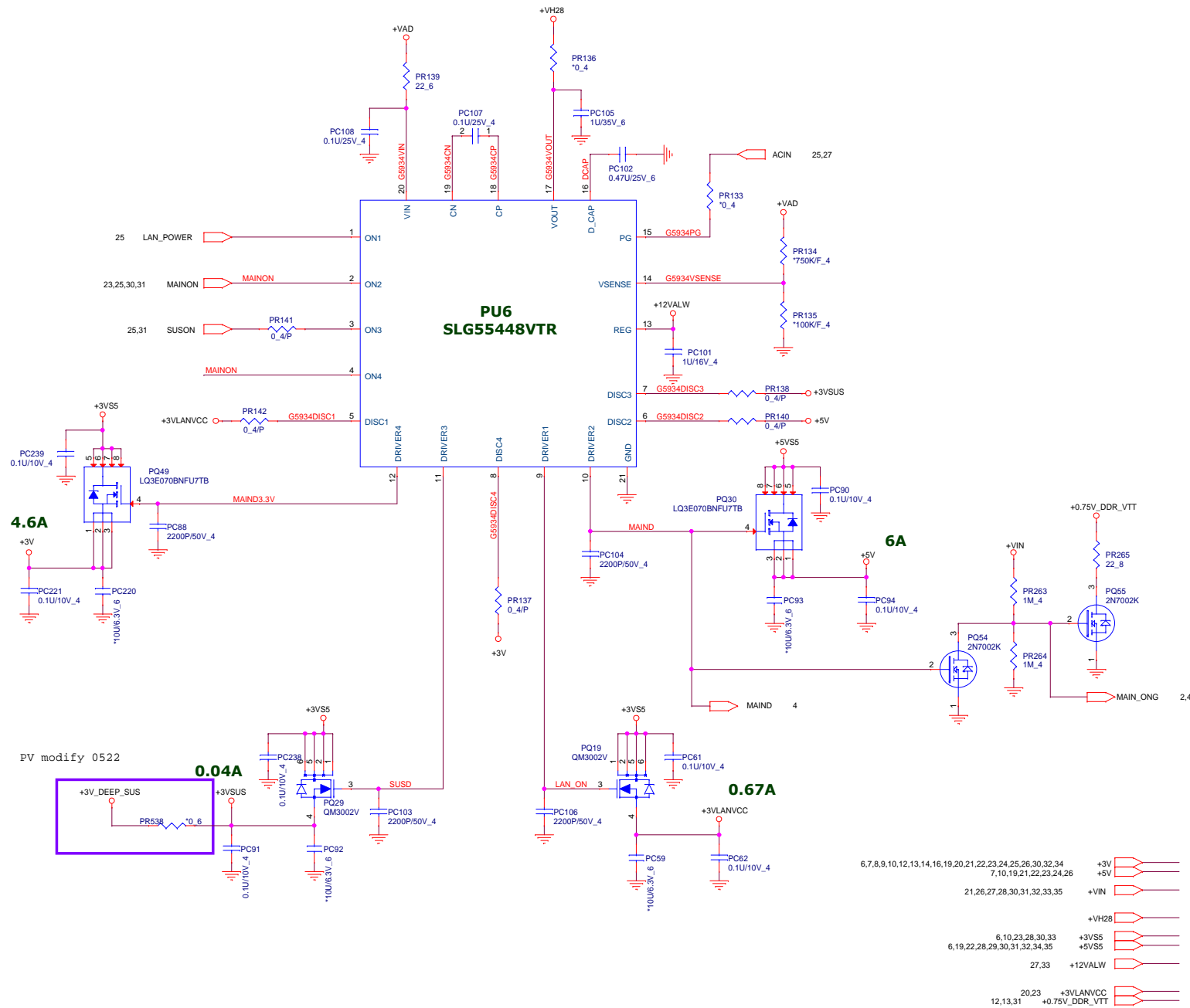
+VCC_CORE (ONLY SUPPORT 35W)

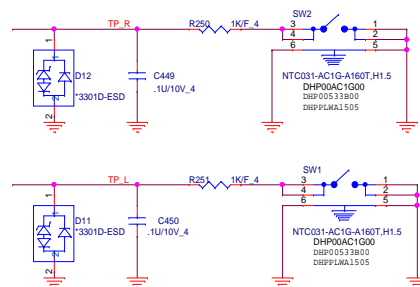
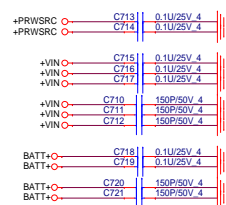
Countinue current:32A
Peak current: 53A
Load Line : -1.9mV/A

+VCC_CORE (ULV 17W)

Countinue current:16A
Peak current: 33A
Load Line : -2.9mV/A





[illegible]